

FORM PTO-1449
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
NIT-83-02

SERIAL NO.

LIST OF DOCUMENTS CITED BY APPLICANT
(Use several sheets if necessary)APPLICANT
Y. SASAKI et alFILING DATE
9/11/00GROUP
2763 2128

U. S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate)
YJ	AA	5,581,202	12/03/96	Yano et al			
	AB	4,477,904	10/16/84	Thorsrud			
	AC	5,144,582	09/01/92	Steele			
	AD	4,541,067	09/10/85	Whitaker			
	AE	5,243,538	09/07/93	Okuzawa et al			
	AF	5,649,165	7/97	Jain et al			
	AG	5,493,504	2/96	Minato			
YJ	AH	4,912,348	3/90	Maki et al			
	AI						
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FOREIGN PATENT DOCUMENTS

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
YJ	AL	4-160569	06/03/92	Japanese Laid-Open Patent				✓
	AM	6-215065	08/05/94	Japanese Laid-Open Patent				✓
	AN	6-20000	01/28/94	Japanese Laid-Open Patent				✓
	AO	7-168874	07/04/95	Japanese Laid-Open Patent				✓
YJ	AP	4-112270	04/14/92	Japanese Laid-Open Patent				✓

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

YJ	AR	INFORMATION PROCESSING SOCIETY OF JAPAN, JOURNAL OF INFORMATION PROCESSING, Vol. 34, No. 5, May 1993, pp. 593-599.
YJ	AS	INFORMATION PROCESSING SOCIETY OF JAPAN, PROCEEDINGS OF 1994 AUTUMN NATIONAL CONFERENCE, Vol. A, p. 64.
YJ	AT	PROCEEDINGS OF IEEE 1994 CUSTOM INTEGRATED CIRCUITS CONFERENCE, 1994, PP. 603-606.

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		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
<i>YJ</i>	AL	1-216622	08/30/89	Japanese Laid-Open Patent				
<i>YJ</i>	AM	1-256219	10/12/89	Japanese Laid-Open Patent				
	AN		//					
	AO		//					
	AP		//					

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

<i>YJ</i>	AR	IEEE TRANSACTIONS ON COMPUTERS, Vol. C-35, No. 8, August, 1986, pp. 677-691.
<i>YJ</i>	AS	PROCEEDINGS OF THE INFORMATION PROCESSING SOCIETY 44TH NATIONAL CONGRESS, PP. 6-143 TO 6-144. <i>no date</i>
<i>YJ</i>	AT	IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-22, No. 2, April 1987. "CMOS Differential Pass-Transistor Logic Design", Pasternak et al, pp. 216-222.

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R. Jones

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9/13/04

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		FILING DATE 9/11/00	GROUP 2763

U. S. PATENT DOCUMENTS

* EXAMINER INITIAL	DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE <i>(If Appropriate)</i>
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FOREIGN PATENT DOCUMENTS

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	AR	IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-25, No. 2, April 1990, "A 3.8-ns CMOS 16 x 16-b Multiplier Using Complementary Pass-Transistor Logic", Yano et al, pp. 388-395.
	AS	IEEE 1994 CUSTOM INTEGRATED CIRCUITS CONFERENCE, 1994 Digest, "Lean Integration: Achieving a Quantum Leap in Performance and Cost of Logic LSIs", Yano et al, pp. 603-606.
	AT	PROCEEDING OF THE 1994 AUTUMN CONVENTION OF THE INSTITUTE OF ELECTRONICS, INFORMATION AND COMMUNICATION ENGINEERS OF JAPAN, Edition of Fundamentals and Interfaces, page 64.

EXAMINER	DATE CONSIDERED <u>9/3/04</u>
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

AR	IEEE TRANSACTIONS ON COMPUTERS, Vol. C-35, No. 3, August 1986, "Graph-Based Algorithms for Boolean Function Manipulation", R. Bryant, pp. 677-691.
AS	DIGEST OF TECHNICAL PAPERS OF IEEE 1995 SYMPOSIUM ON LOW POWER ELECTRONICS, 1995, "Multi-Level Pass-Transistor Logic for Low-Power ULSIs", Y. Sasaki et al, pp. 14-15.
AT	

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	AO					<input type="checkbox"/>	<input type="checkbox"/>
	AP					<input type="checkbox"/>	<input type="checkbox"/>

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AR	Tai: Pipelined-Fault Simulation on Parallel Machines using the circuit flow graph; 1993 IEEE Int. Cont. on Comp. Design; pp. 564-567 10/93
AS	Caban et al.; A parallel BDD engine for logic verification; 5th annual IEEE Int. ASIC Conf., pp. 499-502 19/92
AT	Fujita et al.; Automatic and semi-automatic verification of switch-level circuits with temporal logic and binary decision diagrams; ICCAD-90; pp. 38-41 11/90

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